Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.023 x .023”**

**.035”**

**.035”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .023” X .023”**

**Backside Potential: CATHODE**

**Mask Ref: ZED**

**APPROVED BY: DK DIE SIZE .035” X .035” DATE: 9/1/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .008” P/N: 1N4477**

**DG 10.1.2**

#### Rev B, 7/19/02